Large BGA/SIP Project Discussion

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Agenda

Motivation

Objectives & Inputs

Challenges for substrate surface area + pitch reduction & /IO increase

Current Industry status & roadmap expansion for Motherboard & Die side

Call for interest from membership

Motivation

- **Motherboards are being assembled today.**
- **1.0 and 0.9mm pitch on the MB side –**
- **100-125 micron pitch on die side**
  - **No-Clean & DI process continues on MB side**
  - **Various aqueous & solvents cleaning on die side**
- **Evaluate limit of POR for future assembly**
  - I/O count increase from 10,000 to 20,000 and pitch decreases to 0.4mm
  - Z-height decreases from BGA ball (≥0.75mm pitch) to micro-bump to copper pillar interconnect
    - Each pitch decrease reduces the z-height and tolerance for package warpage
  - Part size (surface area) increases from 100mm sq to 150mm sq and 12omm x 240mm for rectangle.
  - Single die vs. multiple chiplet die - impact to warpage and MB solder joint reliability.

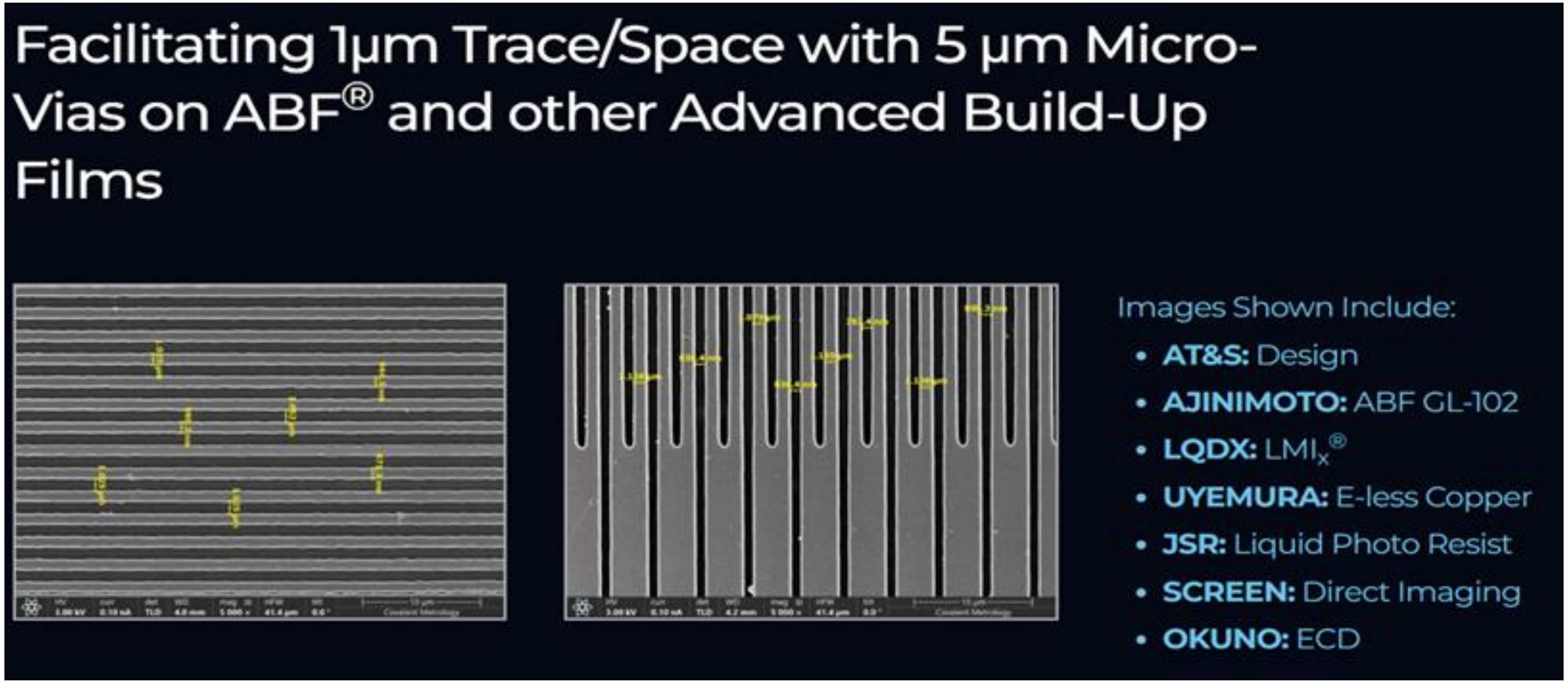
-→→Metal to metal creepage and clearance decreases will increase reliability risk and require mitigation (dendrites, creep corrosion, and leakage current.)

PWB Adv. Substrates

- Density increase 10x – L/S moving from 75 micron to 2-5 micron
  - TLV technology 100 micron to 40-micron laser drilling and Cu plating aspect ratio
  - Embedded and cavity base packages
  - High Density testing and embedded test & diagnostics

Interconnect	Current State	Fanout grid	Roadmap 1-2 yrs	Roadmap 3-4 yrs
BGA Ball – MB Side	0.9mm & 1.0mm pitch	Straight & Staggered	0.6mm	0.4mm
Micro bump Die side	125micron	Straight grid	100 micron	75 micron
Cu Pillar – Die side	75-100 micron	Straight grid	50 micron	<50 micron

LQDX Process



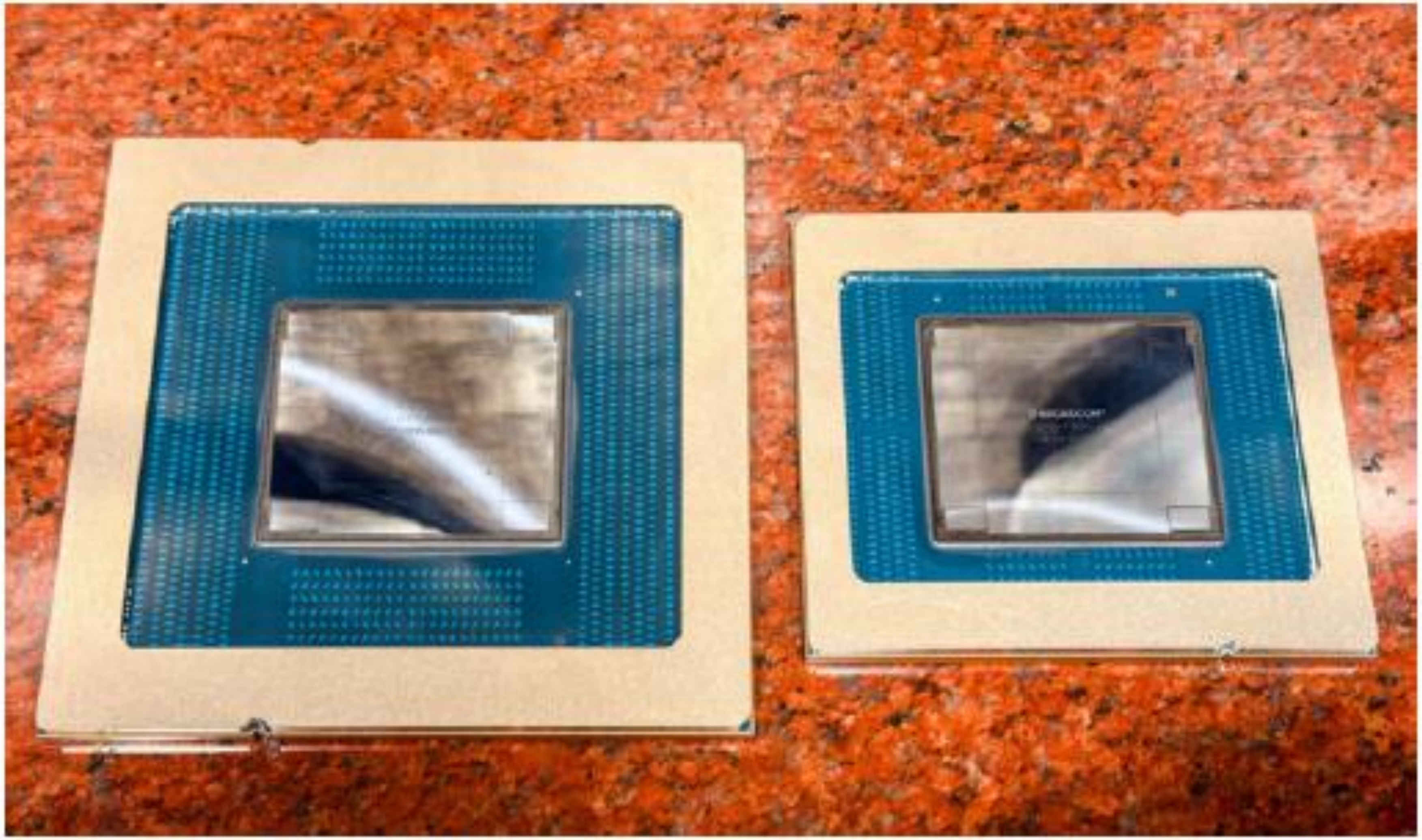
Facilitating 1μm Trace/Space with 5 μm Micro-Vias on ABF® and other Advanced Build-Up Films

Images Shown Include:

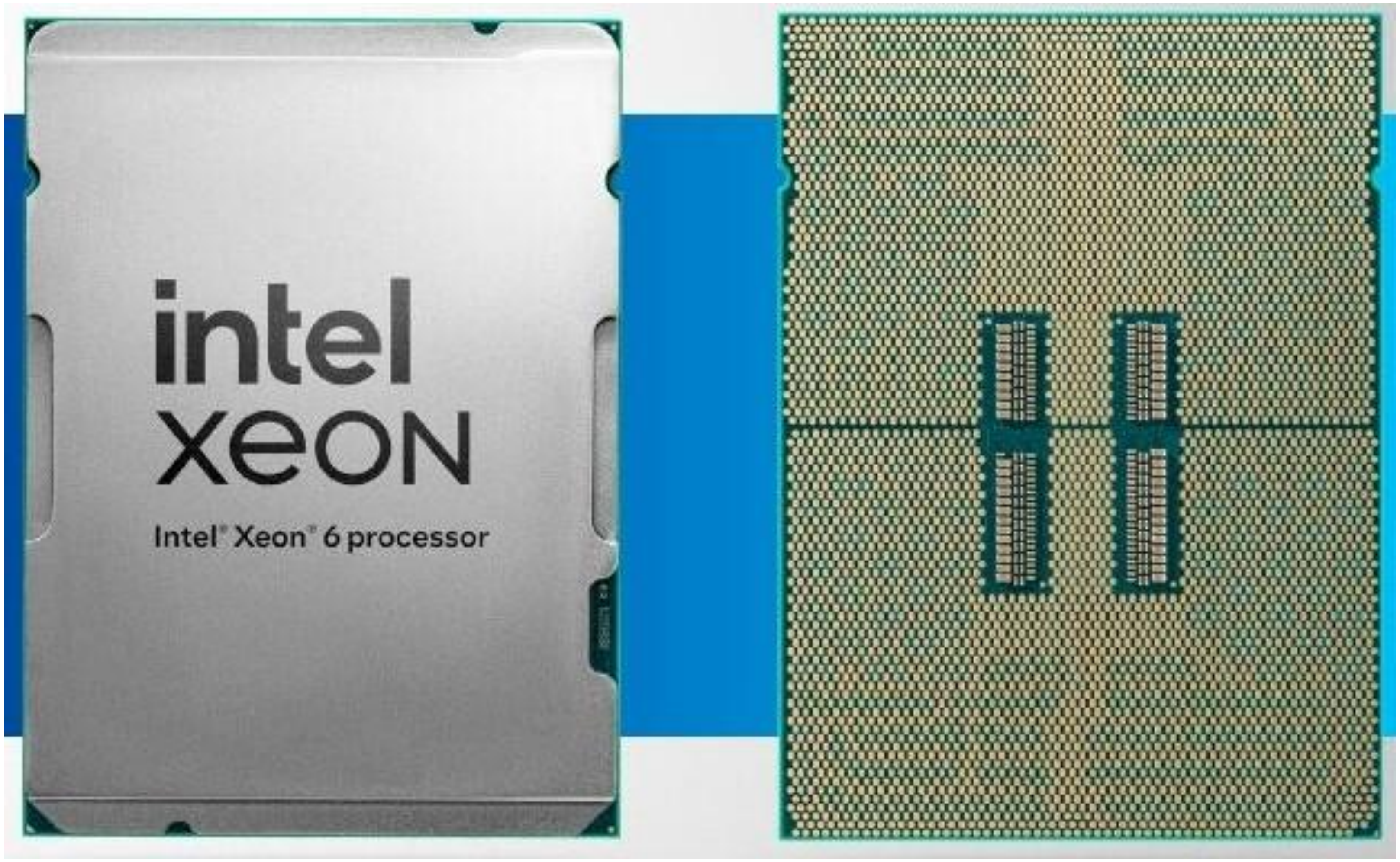
- **AT&S:** Design
- **AJINIMOTO:** ABF GL-102
- **LQDX:** LMI_x®
- **UYEMURA:** E-less Copper
- **JSR:** Liquid Photo Resist
- **SCREEN:** Direct Imaging
- **OKUNO:** ECD

Nvidia

Broadcom

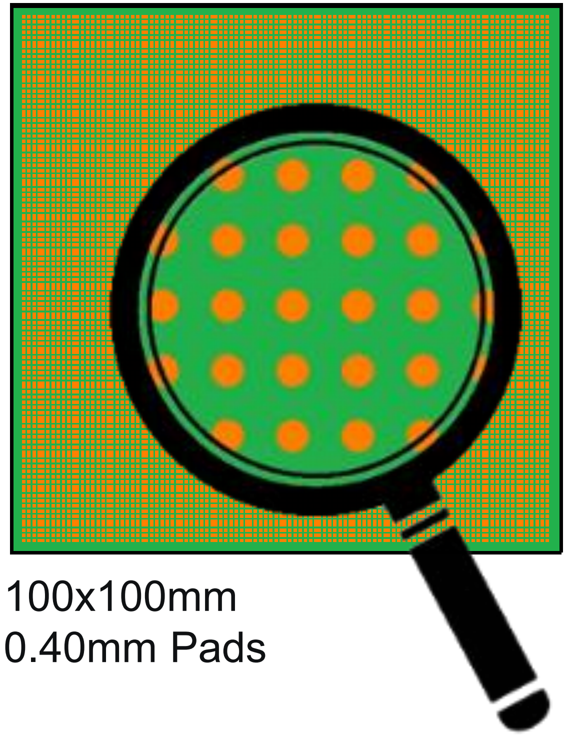


Broadcom Tomahawk 6 112G And 224G SerDes 1


intel
xeon
Intel® Xeon® 6 processor

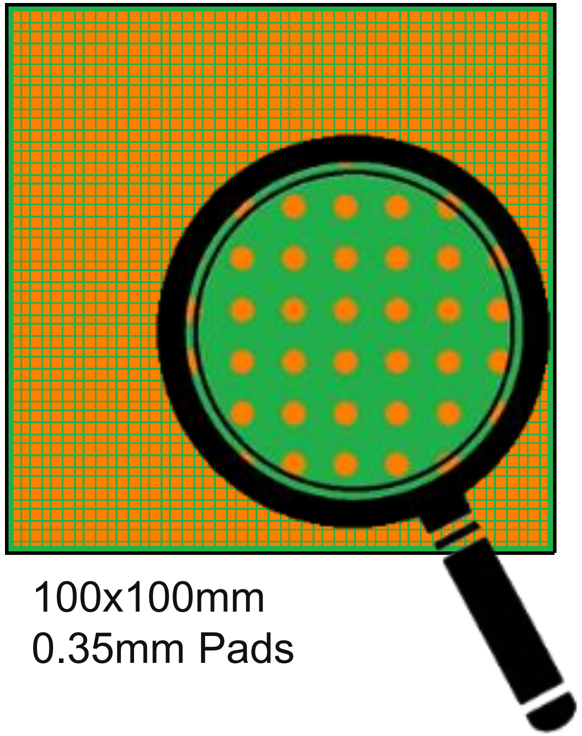
What Will Drive Cost to the Lowest Level?

0.9mm Pitch→ 12,100 I/O



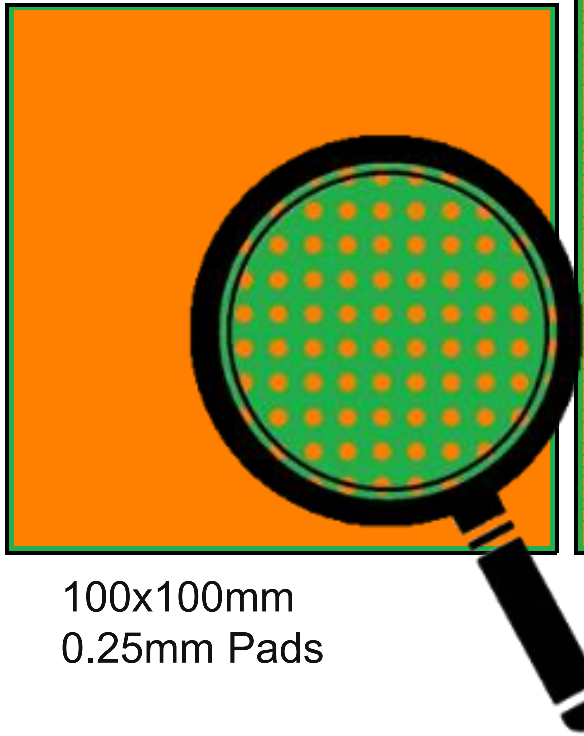
100x100mm
0.40mm Pads

0.75mm Pitch→ 16,900 I/O



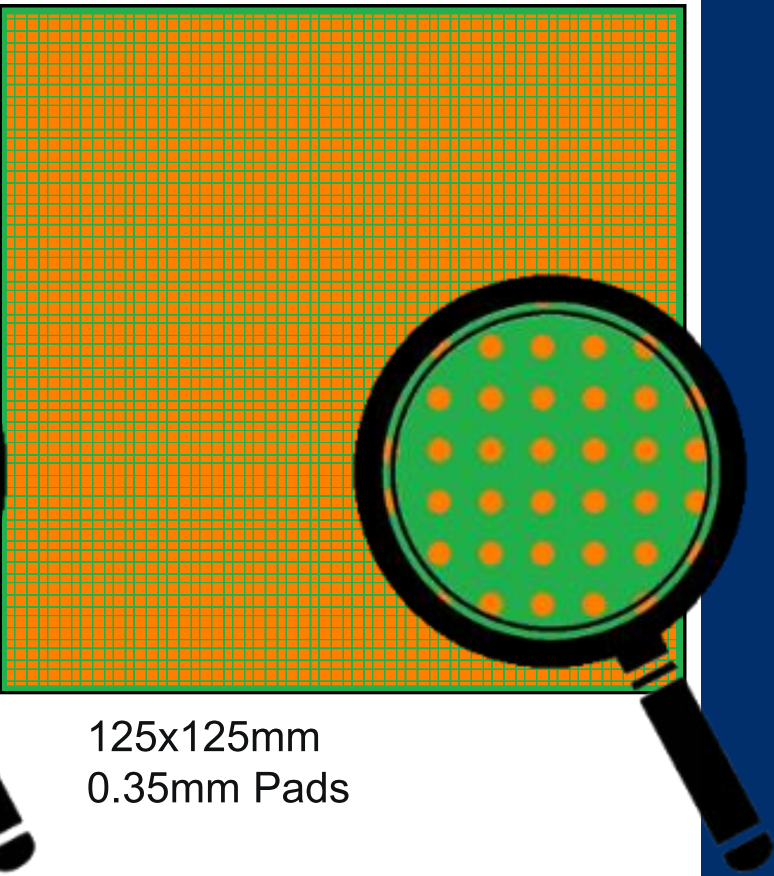
100x100mm
0.35mm Pads

0.5mm Pitch→ 38,025 I/O



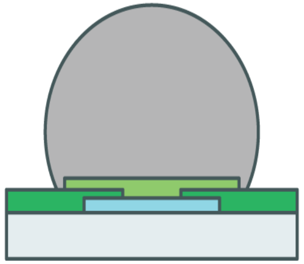
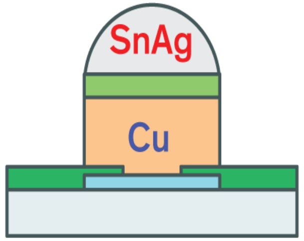
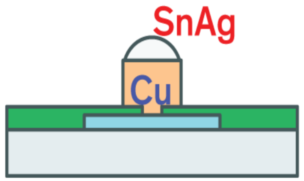
100x100mm
0.25mm Pads

0.75mm Pitch→ 26,569 I/O



125x125mm
0.35mm Pads

Wafer Cu Pillar Process Motivation

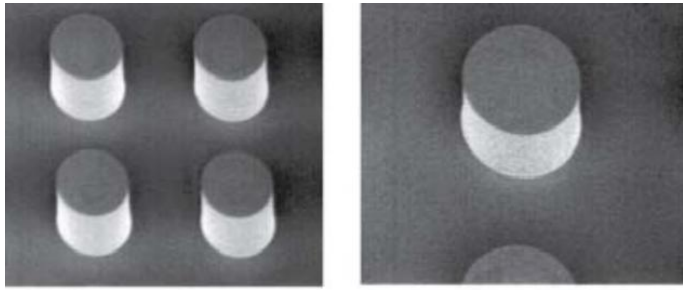
	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu μ-Pillar + Pb-free Cap
Structure				
Diameter	75 – 200 µm	75 – 150 µm	50 – 100 µm	10 – 30 µm

Old Technology

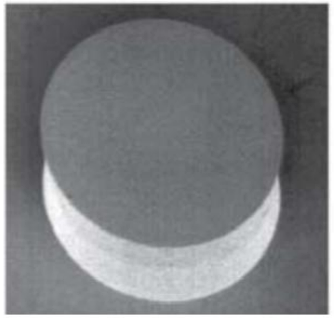
Current Technology

Next-Generation Technology

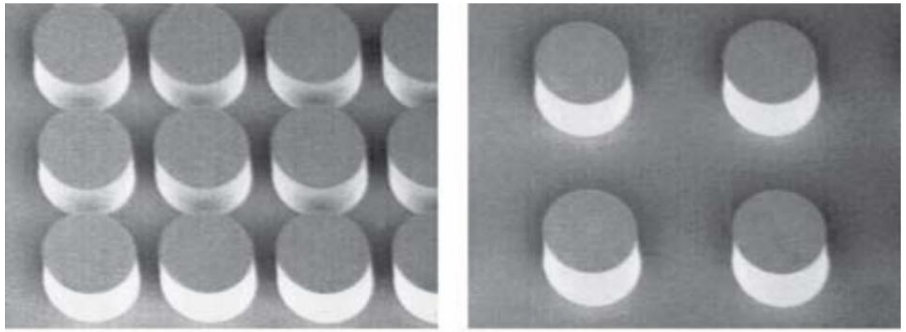
Cu Pillar Images



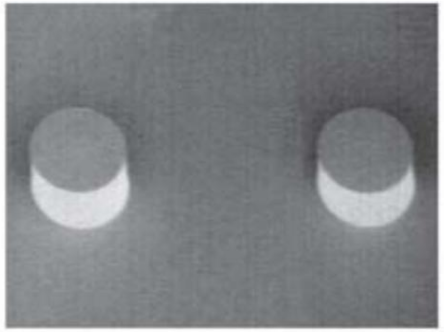
(a) 30 µm pillar (b) 50 µm pillar



(c) 100 µm pillar



(a) 12.5 µm spacing (b) 50 µm spacing



(c) 100 µm spacing

Characterization of a Thick Copper Pillar Bump Process Warren W. Flack, Ha-Ai Nguyen Ultratech, Inc.
San Jose, CA 95126 Elliott Capsuto, Craig McEwen Shin-Etsu MicroSi, Inc. Phoenix, AZ 85044

Motivation – Additional Reliability Study Areas

- Laminate vs. glass/silicon vs. ceramic substrates – Fan-out, RDL layer count, warpage and cost related factors.
- Part placement strategy development –
  - Part weight limitations for Pick & Place (Parts >300 grams now)
  - Fiducial strategy for alignment in P&P
  - Die side ball attach process/cu pillar attach processes printing limits?
- Warpage Measurement ties to alloy selection depending on cu layer stack-up & % cu remaining.
- Forced rework evaluation – how to deal with various process elements; removal, site dressing, flux/paste replacement on large areas >100mm sq, hot air reflow profile impact on part warpage & reliability of reworked parts.
- Summarize positions on electrical current density and impact on LTS alloys– summarize current state from prior work (BEOL Package houses & Enterprise computing OEM’s).

Objectives & Inputs - for Project Plan Consideration

- Working with iNemi to jointly manage. Definition of technical ‘swim-lanes’ and parallel lane runs to accelerate time to solution.

- 4 joint iNemi/UIC meetings to date – open to public for project inputs now.

- Contact Dave or Jeff for getting connected. Definition of scope and leaders and priorities being discussed now.

Objectives & Inputs - Areas for Consideration

Possible parallel technology lanes: Definition of project scope & priorities for pre-competitive work related to manufacturing assembly and reliability.

- Cleaning and baseline residue analysis – Zestron & UIC APL
- Member supplied test parts – Ionic Contamination & Cleaning at Zestron through UIC APL.
- Laminate vs. glass/silicon vs ceramic substrates – OEM input on TCOO of each.
- Test Vehicle definition for Soldering, mechanical & accelerated reliability tests – UIC APL
- Thermal Moire warpage analysis and Design Rule BKM definition – Single and multiple die
- Substrate Carriers (Pitch & surface area matrix) for MB screening tests for cleaning - Zestron & UIC APL
- Part placement & Assembly strategy – UIC AREA & APL
  - Part weight limitations for P&P (Parts >300 grams now)
  - Fiducial strategy for alignment in P&P
- Reliability studies with & without ruggedization
- Validation of roadmap – From OEM’s
- Forced Rework study on localized cleaning and accelerated reliability tests
- Fluid flow analysis and modelling
- Studies for ruggedization; corner bond, edge bond, molded underfill, traditional underfill
- Thermal & mechanical robustness enhancement
- Evaluation of optical and digital integrated modules

Design of Test Vehicles

➢ *Note: Package and Board Test vehicles are not available today for Large FF BGA assessment. Procurement of actual Large FF BGAs from OEMs will be very difficult and expensive.*

Attribute	Package	PCB
Design Considerations	**Form Factor Size** • 120 mm x 120 mm proposed • But other sizes also feasible **Die/Chiplet Size and Layout** • TBD **Daisy Chain connections** • Multiple daisy chains with corner joints and die shadow joints in differentiated **Ball Pitch and Diameter** • Obtain information from all current Large FF BGA products and pick median values **Substrate Thickness and Stack-up** • Obtain information from all current Large FF BGA products and pick median values **Substrate Laminate** • BT or other most prominent laminate in use for LFF BGAs **Substrate Surface Finish** • ENIG is prevalent • OSP and ENEPIG are alternates **Substrate Land Design** • Solder mask Defined	**Size (X-Y)** • 305 mm x 305 mm • Does IPC 9701 Rel Spec specify a size? **Daisy Chain connections** • Mirror connections on the package substrate **Land Pitch and Diameter** • Mirror Pitch on the package and use IPS-7095 recommendation for diameter **Thickness and Stack-up** • Obtain information from all current Large FF BGA product PCBs and pick median values **Substrate Laminate** • FR-4 or other most prominent laminates in use for LFF BGAs **Substrate Surface Finish** • OSP is prevalent • ENIG and ENEPIG are alternates **Substrate Land Design** • Solder mask Defined or Non-solder mask Design **Routing out Failed Packages** • capability to route out any single component after failure

Fabrication/Assembly of Test Vehicles

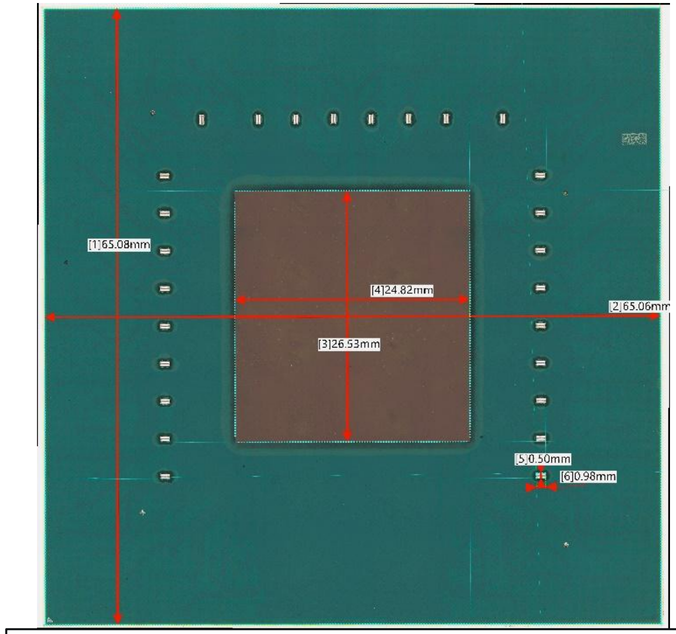
- ➢ *Note: Package and Board Test vehicles are not available today for Large FF BGA assessment. Procurement of actual Large FF BGAs from OEMs will be very difficult and expensive.*

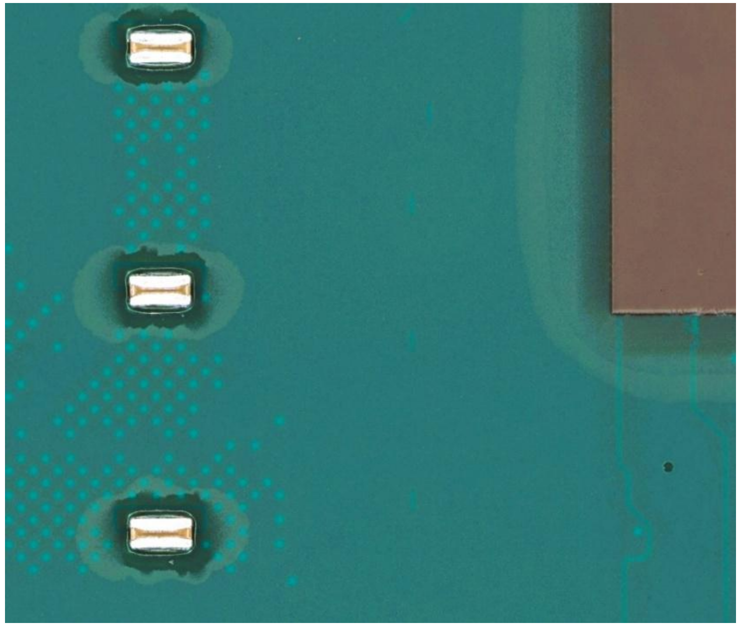
Attribute	Package	PCB
Fabrication Considerations	**Substrate Supplier** • One of the current BGA substrate suppliers in the industry o Shinko o Ibiden o ATS o Nanya o Other **Solder Alloy for Spheres and Ball Attach** (possible alternatives) • SAC305 • High Rel SAC • Medium Temp Alloy • Low Temp Alloy Note: Flux only is a possibility for Ball Attach **Ball Attach Assembler** • Canvass various industry Ball Attach houses for capability and line time availability for Ball Attach • RIT also a possibility	**PCB Supplier** • Use INEMI preferred supplier or the most popular suppler in the DC AI PCB market currently **Solder Paste Alloy for Spheres** (possible alternatives) • SAC305 • High Rel SAC • Medium Temp Alloy • Low Temp Alloy • Note: Each alloy composition may have a different supplier **Board Assembly House** (possible alternatives) • RIT • Intel Kulim (Malaysia) • INEMI preferred ODMs

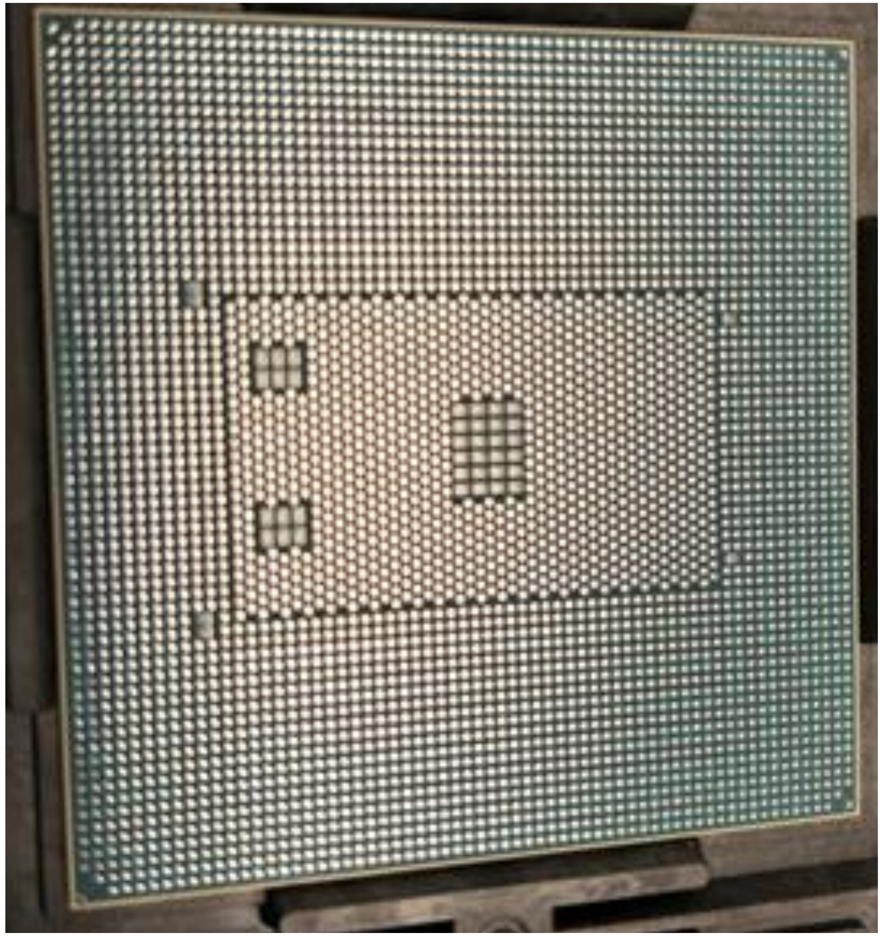
Experimental Design Considerations

Attribute	Assembly Process Development	Accelerated Temperature Cycling Reliability
Experimental Design Considerations	**Package Dynamic Warpage Measurement Solder Alloy for Spheres and Ball Attach** • Using Shadow Moire Process **DOE Variables** • Solder Paste • Reflow Profile Critical Parameters • Stencil Apertures • Reflow Oven Atmosphere **Data Collection and Analysis** • Solder Joint Yield ○ Based on daisy chain resistance measurement (time 0) and confirmed with visual /X-ray Inspection • Solder Joint Void Content • Solder Joint Microstructure • Solder Joint Height **Underfill / Corner Glue Process** • Underfill Type and Suppler ○ Zymet ○ Other ▪ Interaction with Solder Paste Flux Assessment ○ Pull Test Post Glue Curing process	**Temperature Cycling Protocol** • 0 to 100 C (Standard, baseline for INEMI Projects) • Other alternatives if warranted • Standard electrical resistance monitoring of solder joints using daisy chain connections • Standard Event Detectors **Failure Analysis** • Routing Failed packages/ • preparation for XS, • XS and Polish, • Inspect in OM and SEM **Data Analysis** • Weibull Plots

OEM Parts for Baseline Discovery







Top side:

25mm sq. die with 100 micron pitch micro-bump SAC305
0201 decoupling capacitors on periphery.

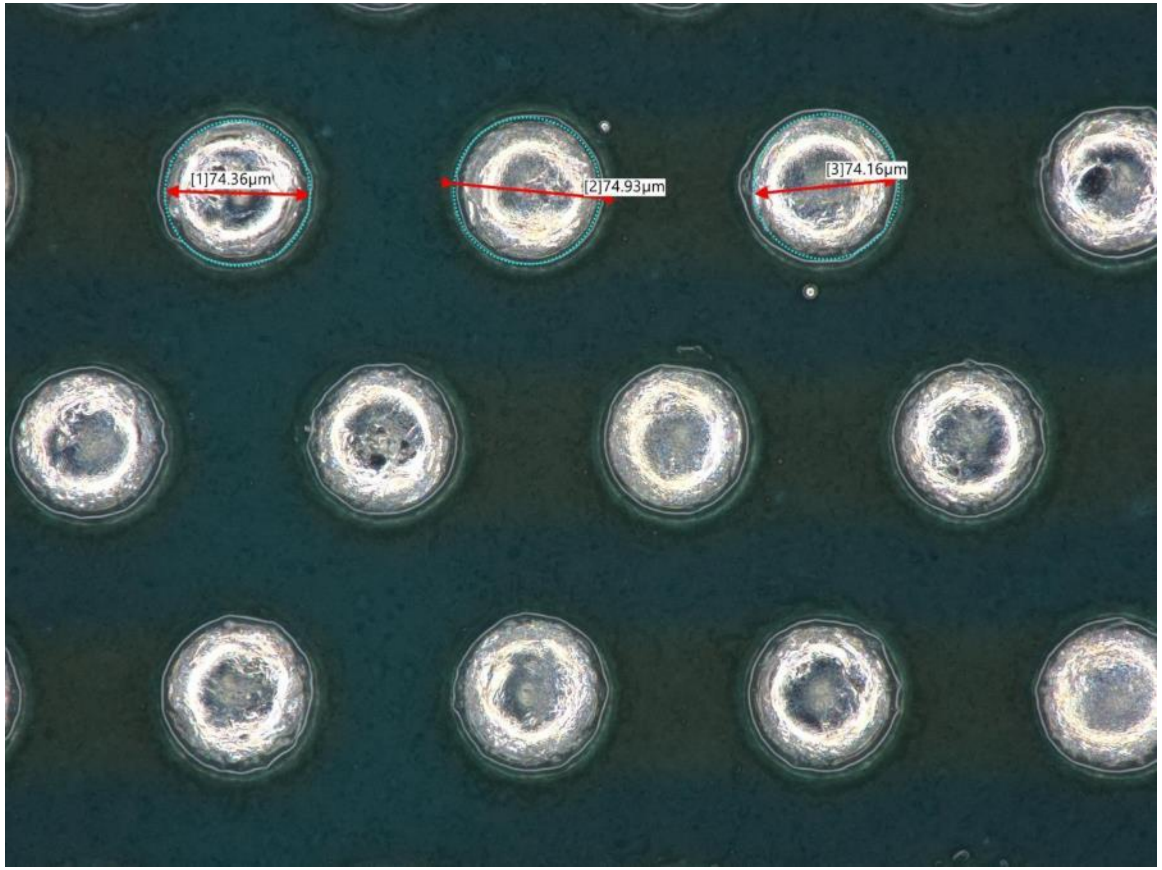
Bottom side:

0201 between the 1.0 mm pitch solder balls – tricky SMT process? Note staggered grid + Straight grid fan-out pattern

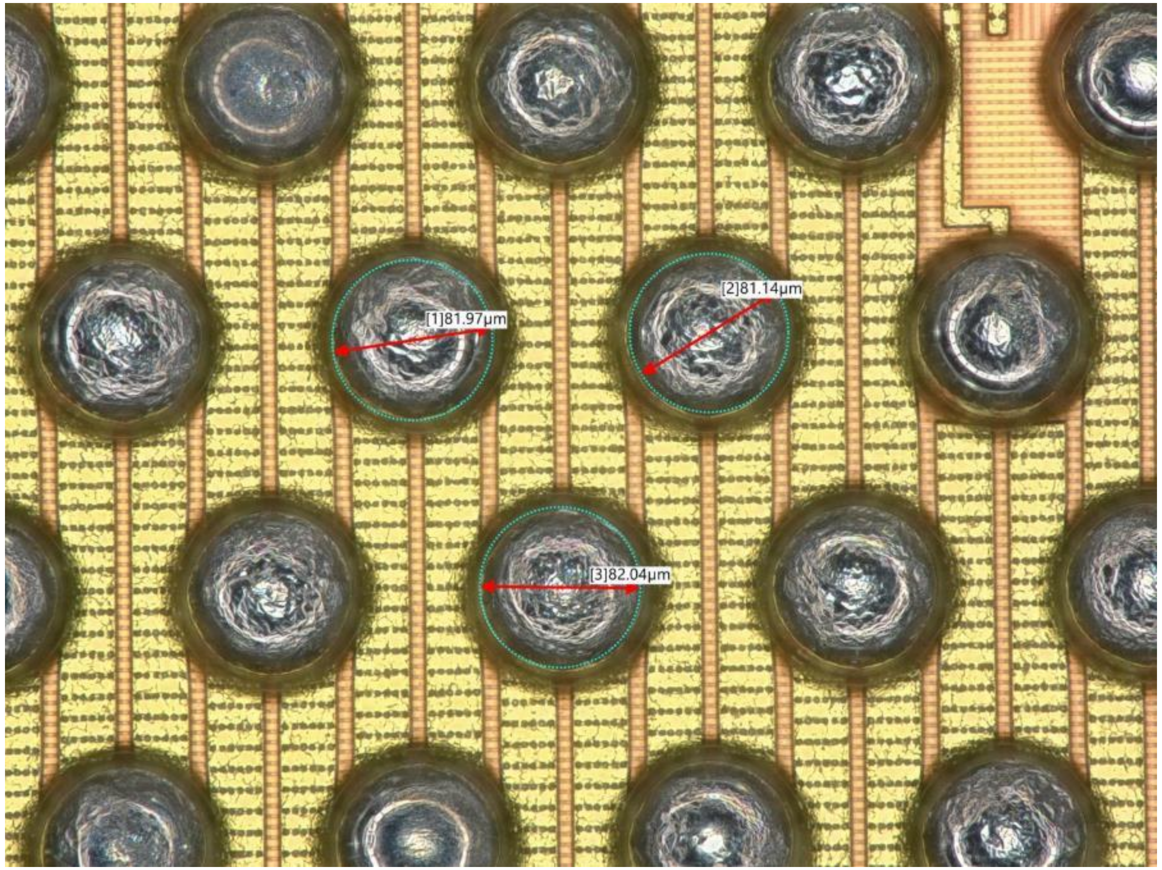
Other member parts/test vehicles?

C

Optical Images of Sample After Reflow



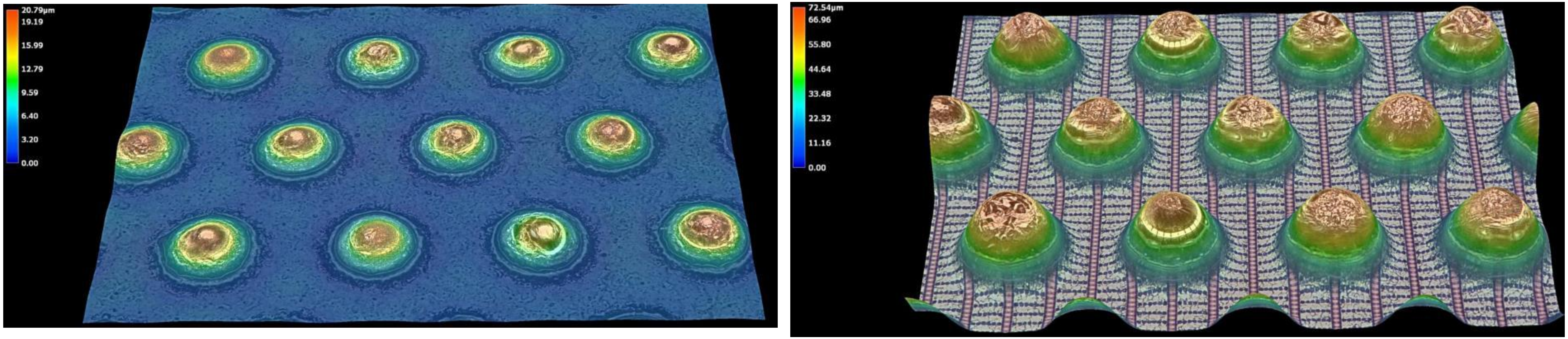
PCB



Device

Solder bump / pad diameters measured on the PCB and Device were 75 and 82 micrometers, respectively.

Optical Images of Sample After Reflow

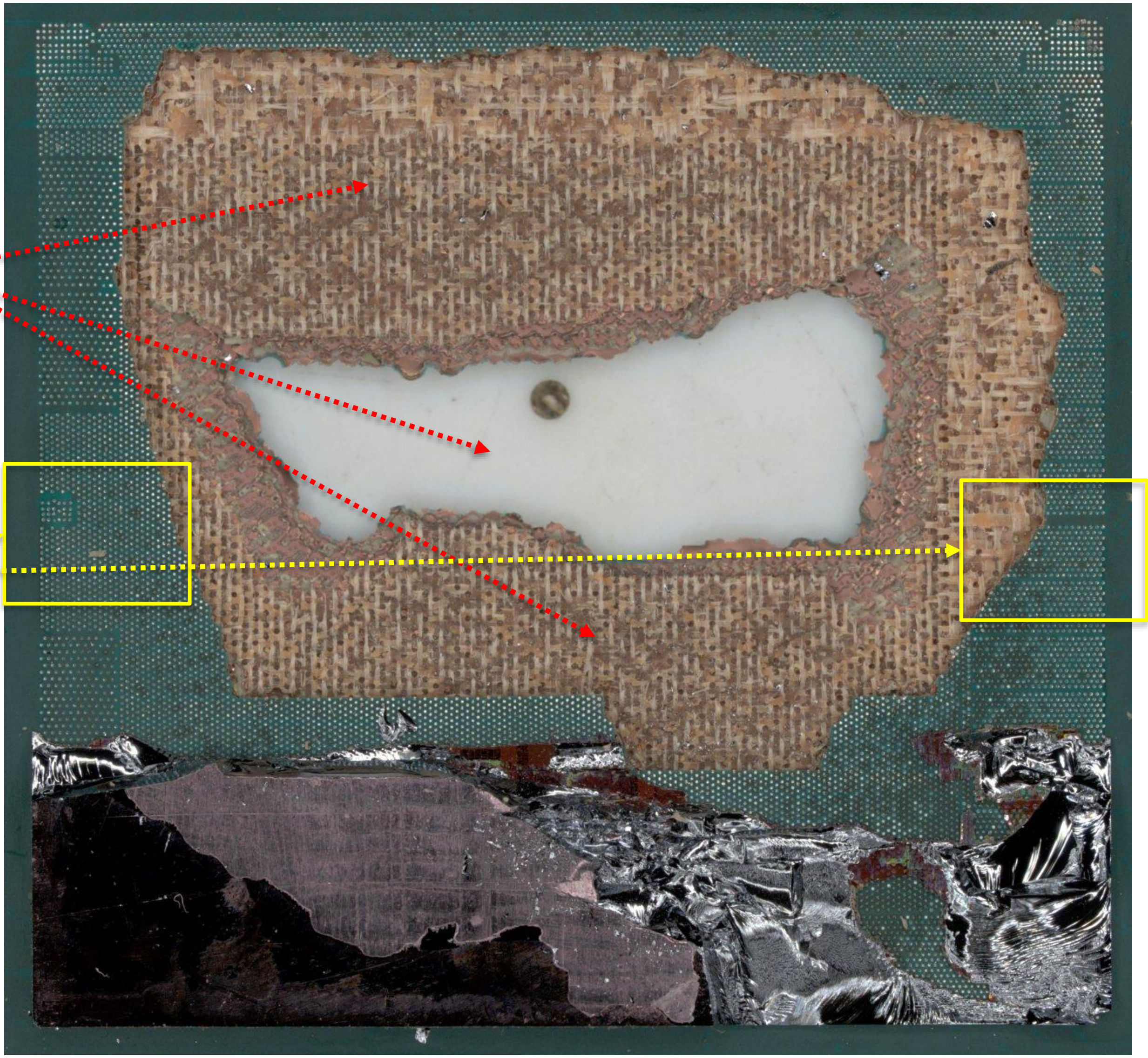


PCB

Device

3D optical reconstruction images of the solder bumps in the center region on the PCB and Device.

Optical Images of Sample 2 After 1st Pull Attempt



PCB Fracture

SEM Imaging

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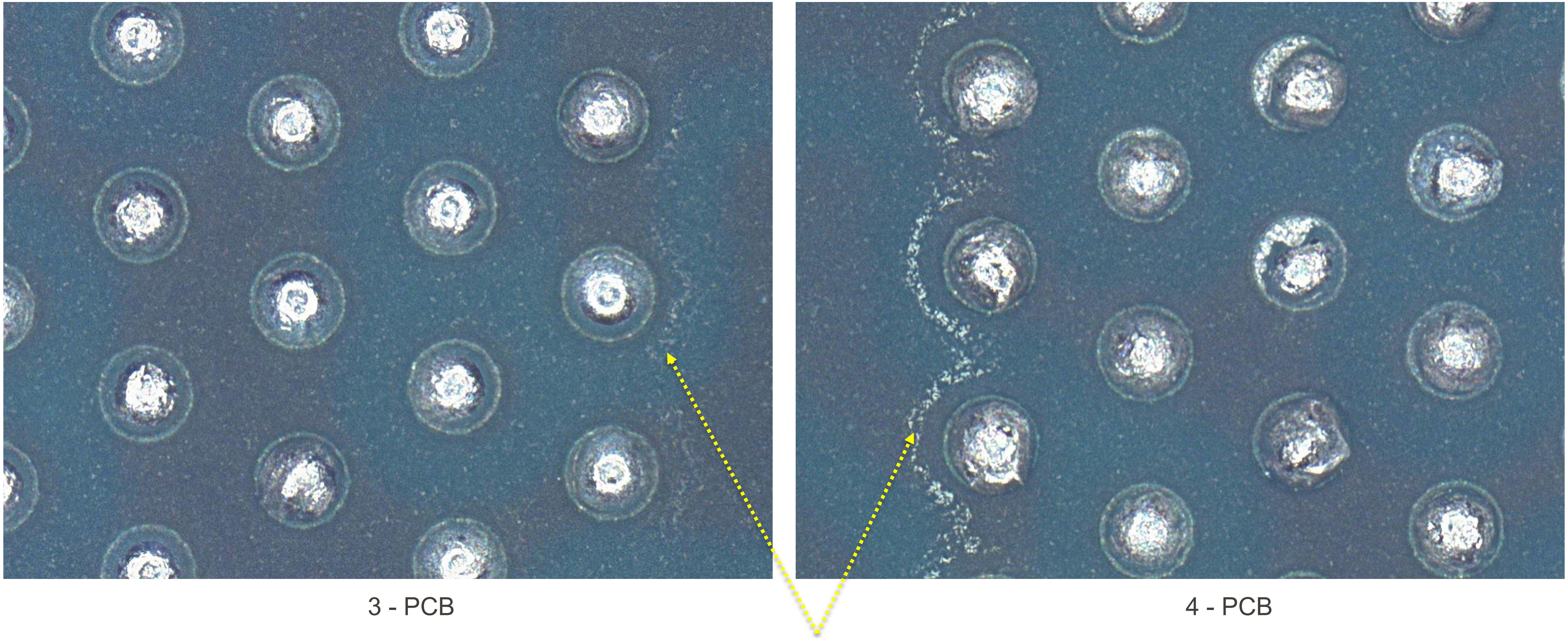
Optical Images of Sample 3 and 4 After Reflow

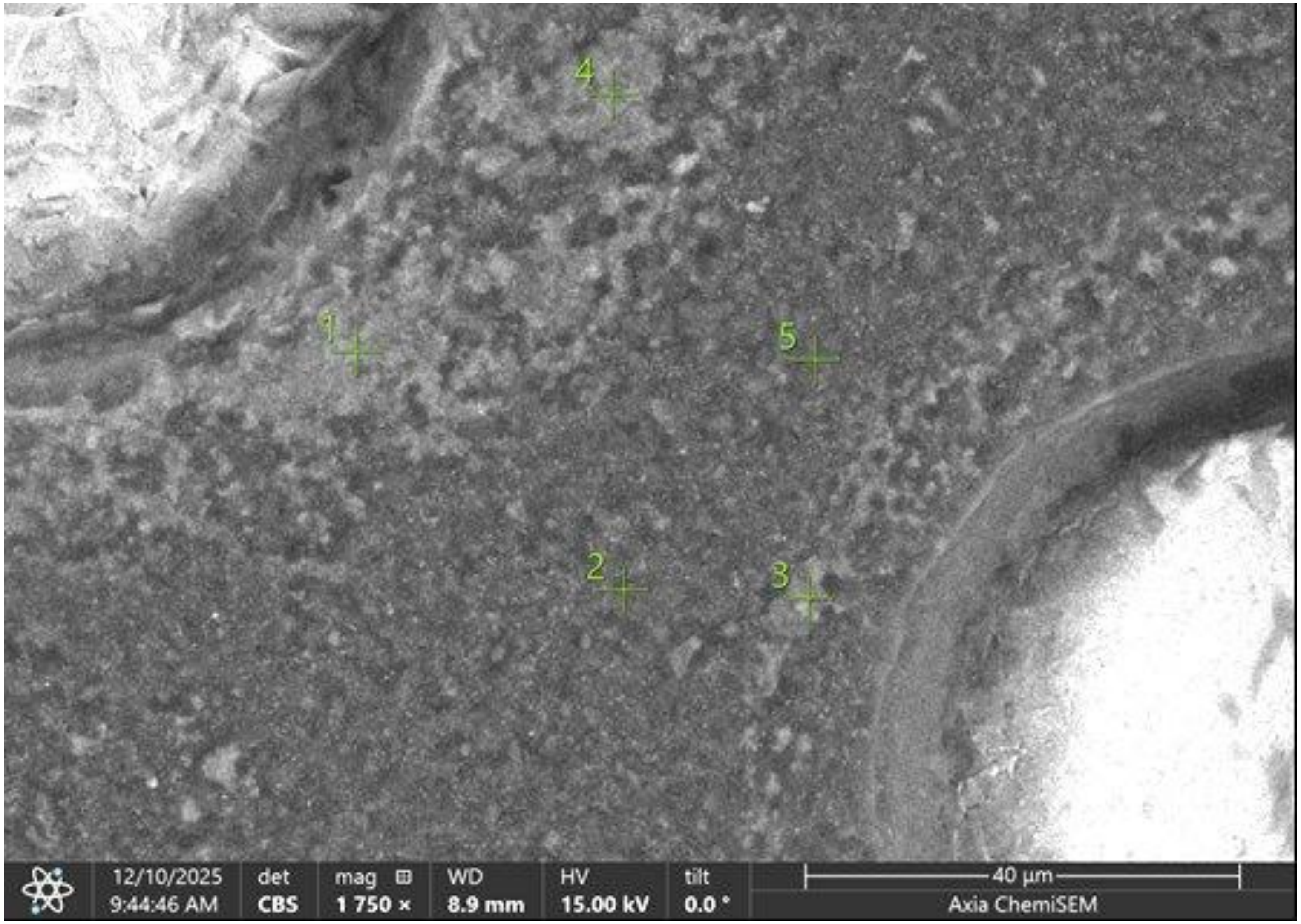


3 - PCB

4 - PCB

Residue

EDS Results from Sample 2 After Pull

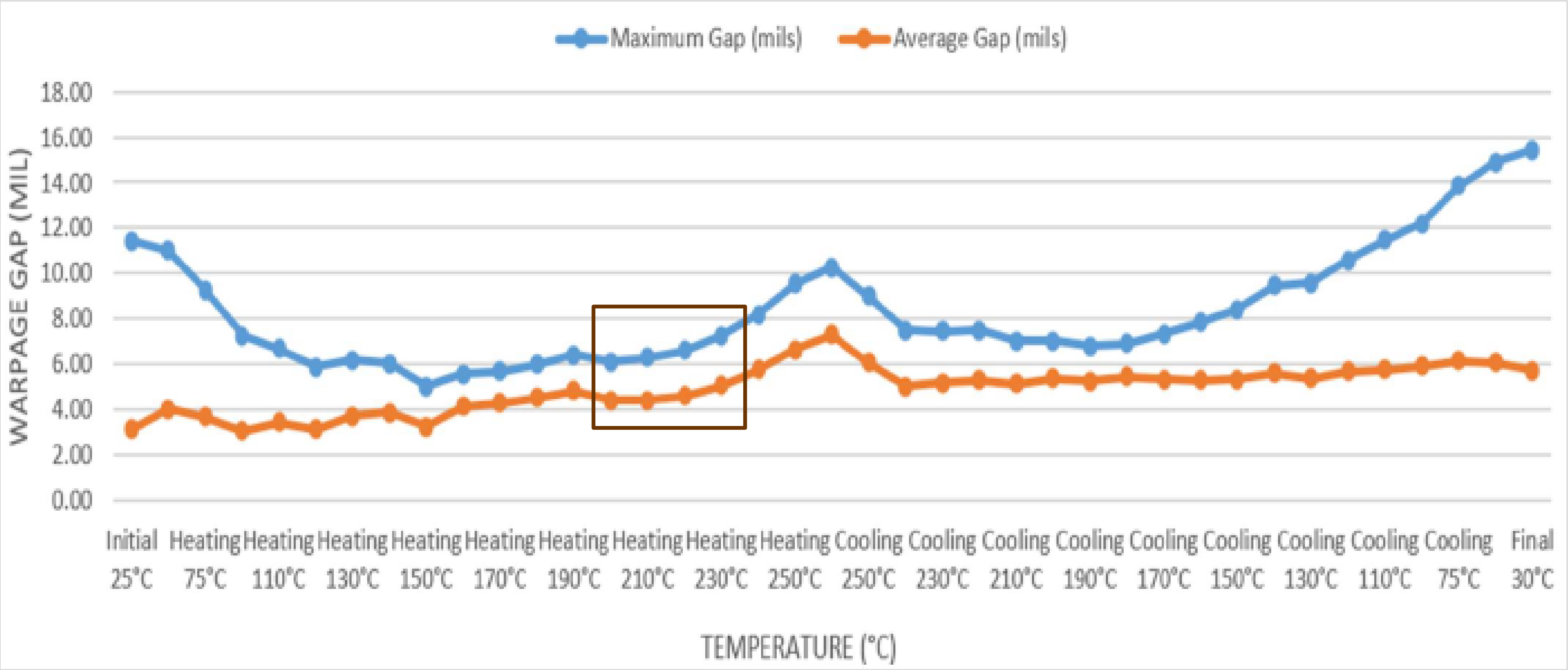


	Weight %				
Element	**Point 1**	**Point 2**	**Point 3**	**Point 4**	**Point 5**
C	24.8	35.4	25.5	26.4	34.8
N	3.2	0.0	3.7	3.6	0.0
O	34.2	32.0	30.7	33.0	31.8
Al	0.9	0.7	0.8	0.7	1.4
Si	1.7	4.7	3.0	2.1	4.0
S	0.7	3.1	1.7	0.6	2.7
Cl	2.4	1.1	2.2	2.5	1.3
Sn	32.1	11.0	25.9	27.0	13.3
Ba	0.0	12.0	6.5	4.1	10.7

Note Sn dissolution into the gap

→Risk of leakage current

Warpage Interface Analysis



Next Steps

- Get member feedback on interest of project.
- See if any member parts, dummy parts are available for screening tests.
- Identify willing known sources for test substrates and copper pillar plating.
- Get screening test vehicle and glass parts for cleaning evaluations – design work 90% completed. Suppliers discussions under way.
- Develop Project scope document with iNemi.
- Get outline and write project proposal with member inputs ongoing now. Get involved!
- Confirm parallel lanes and SME’s to lead each.

Acknowledgements

The authors would like to recognize contributions by UIC Advanced Process labs in the baseline package evaluation and support of project development initiatives going forward.

- David Vicari Vicari@uic.com
- Michael Meilunas meilunas@uic.com
- Dan VanHart Daniel.VanHart@uic.com

Thank-you for your time and attention!